

FIG. 1

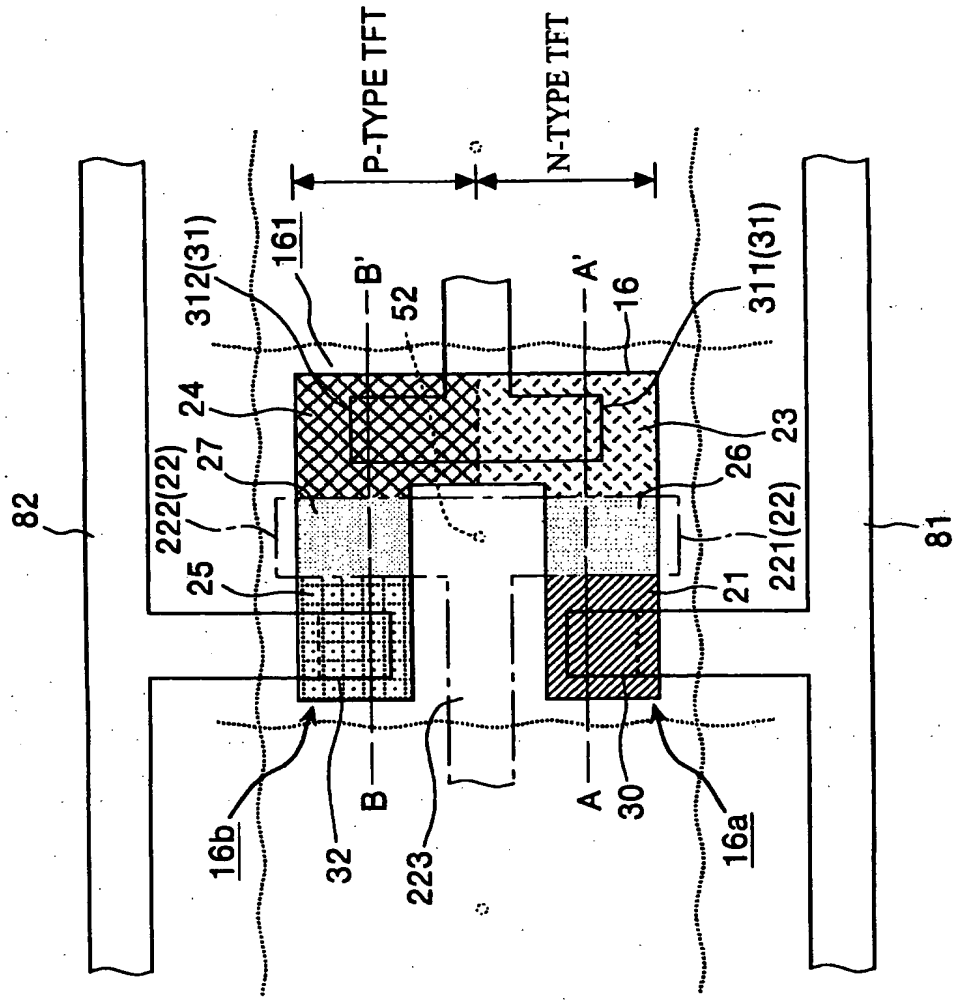


FIG.2

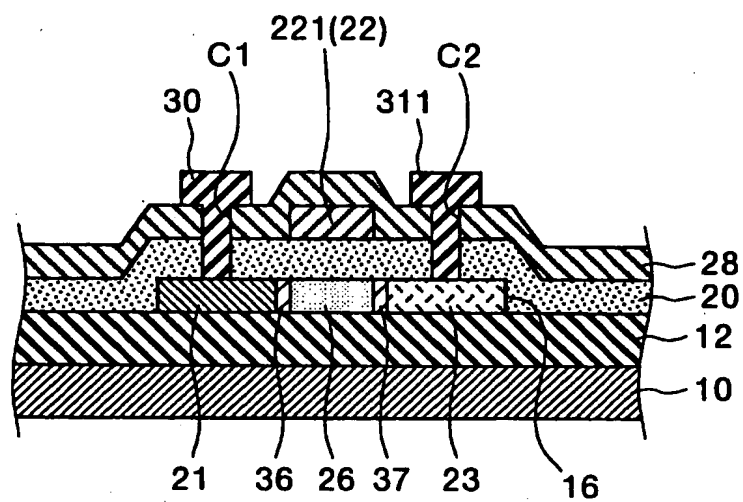


FIG.3

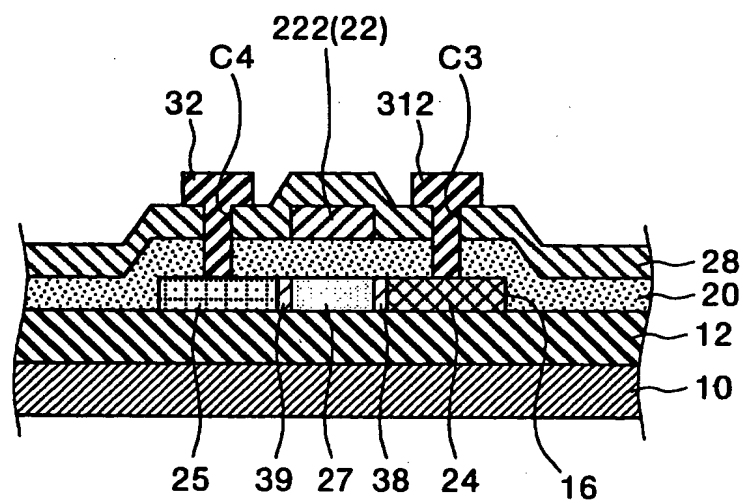


FIG.4

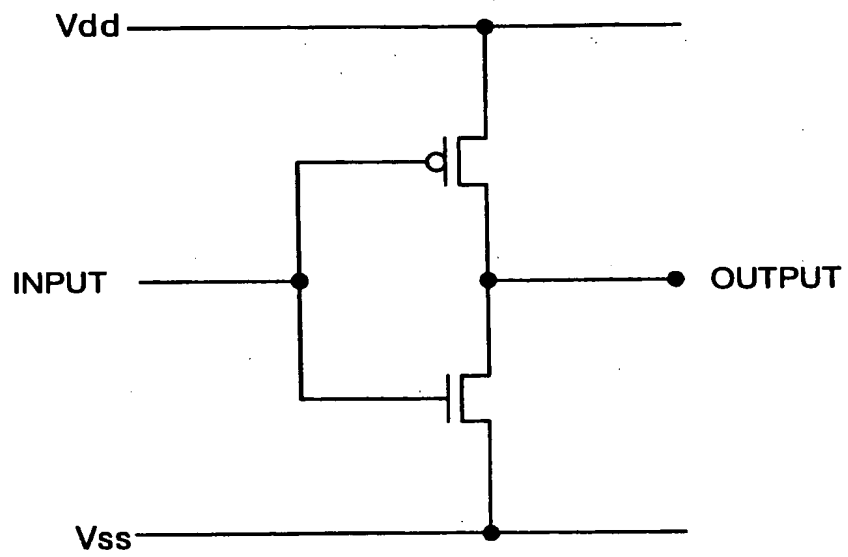


FIG.5

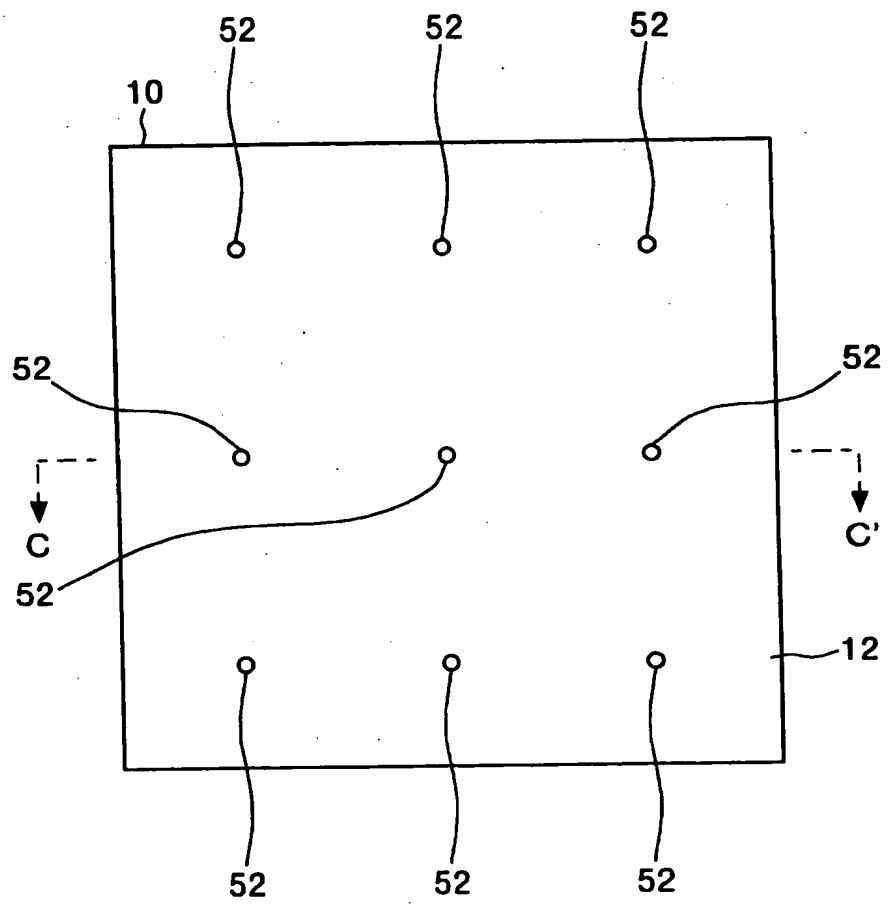


FIG.6A

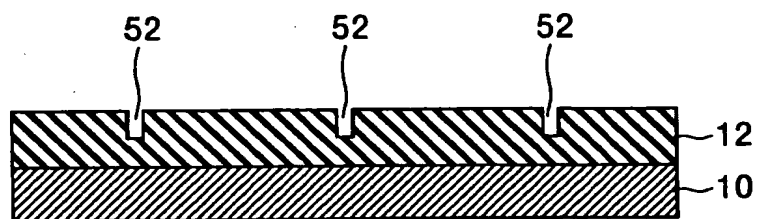


FIG.6B

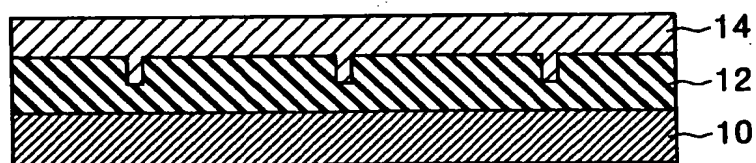


FIG.6C

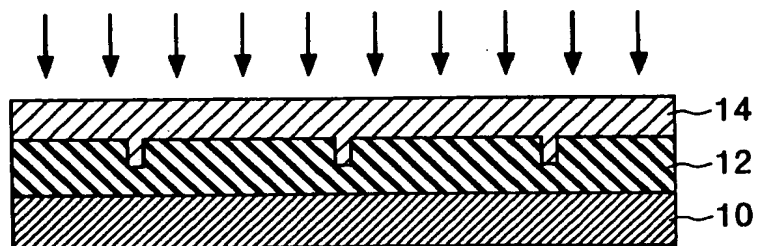


FIG.6D

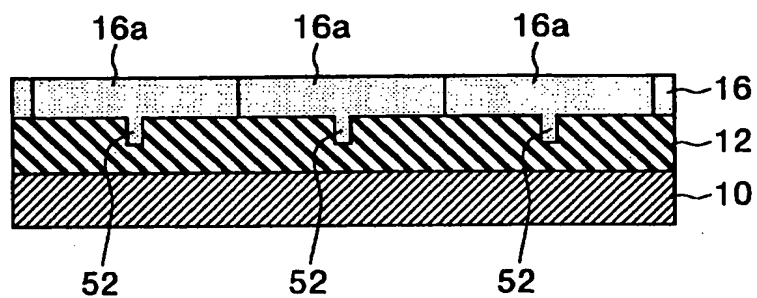


FIG.7

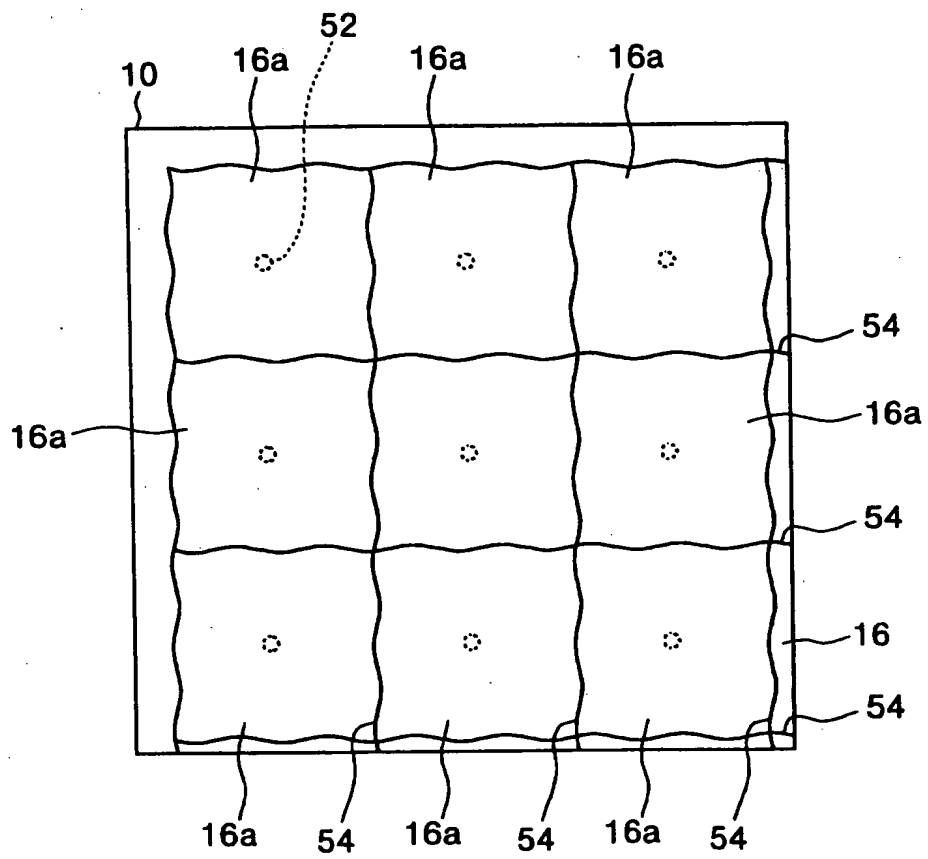


FIG.8

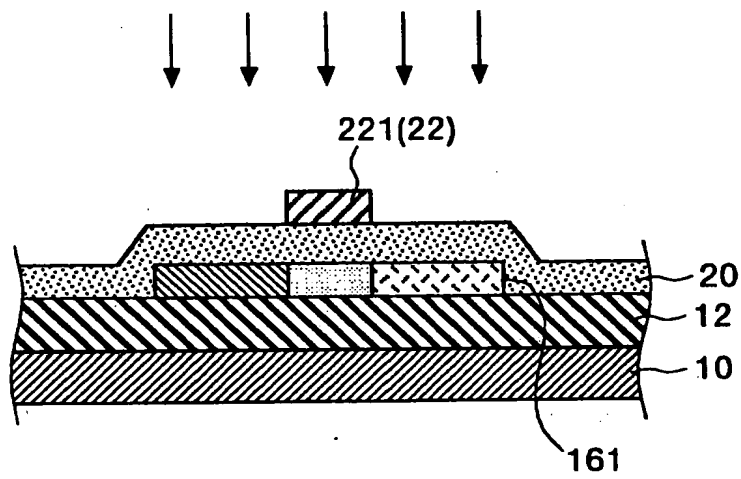


FIG.9

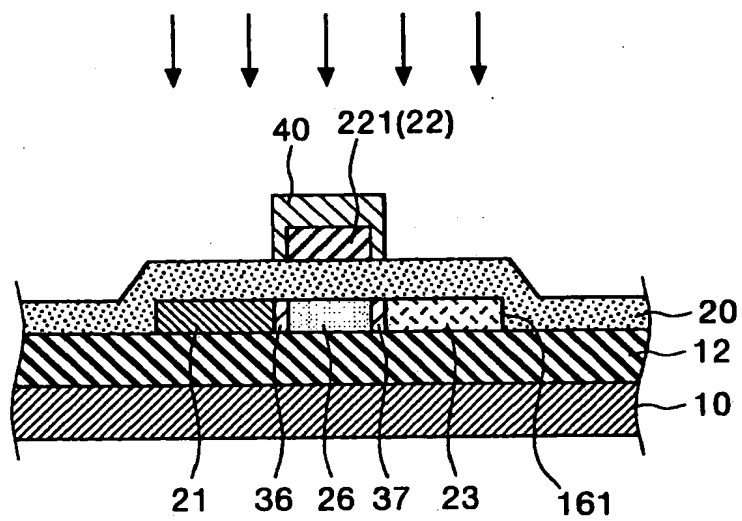


FIG.10

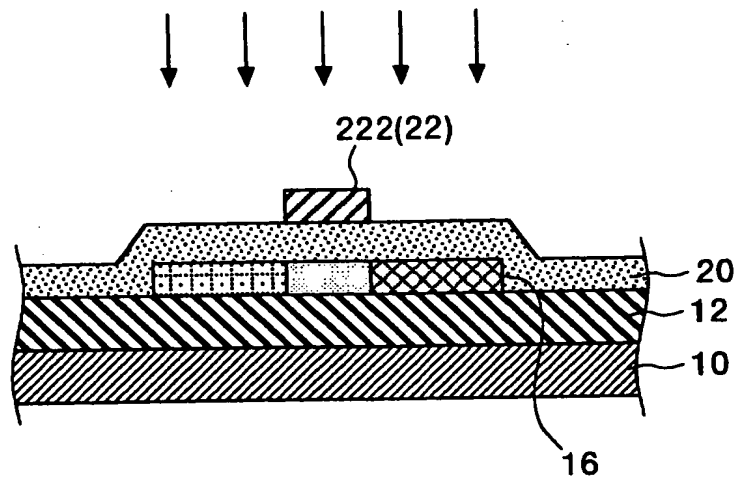


FIG.11

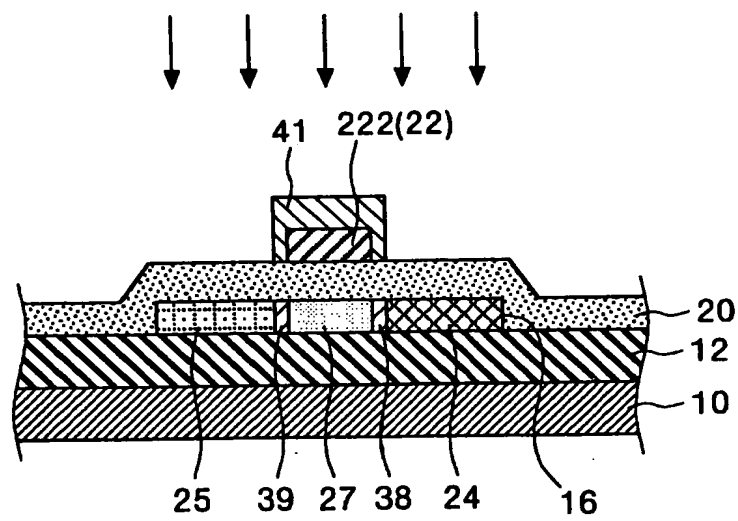




FIG.12

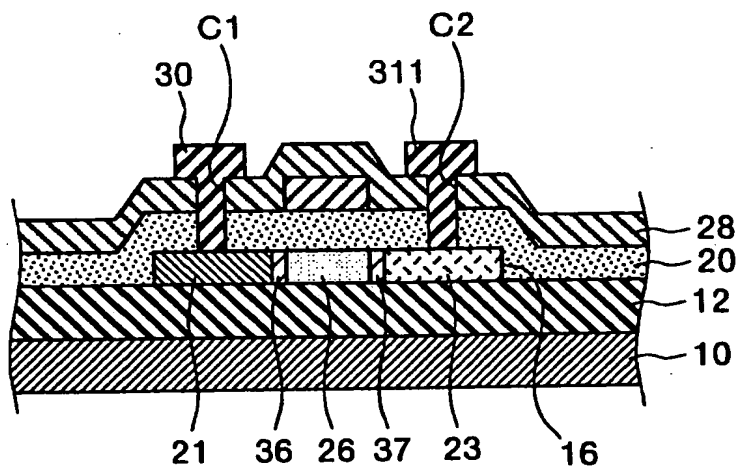


FIG.13

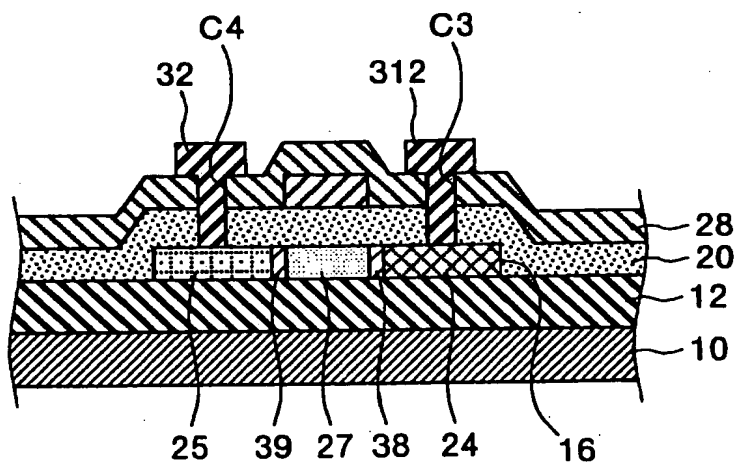


Figure 1 is a plan view of a semiconductor device. The device is divided into four quadrants by a vertical line 16a and a horizontal line 16b. The top-left quadrant contains a central square region 30, surrounded by a patterned region 23, which is further surrounded by a region 26. The top-right quadrant contains a central square region 31, surrounded by a patterned region 23, which is further surrounded by a region 26. The bottom-left quadrant contains a central square region 30, surrounded by a patterned region 23, which is further surrounded by a region 26. The bottom-right quadrant contains a central square region 31, surrounded by a patterned region 23, which is further surrounded by a region 26. The device is divided into four quadrants by a vertical line 16a and a horizontal line 16b. Dimensions P1, N1, P2, and N2 are indicated. Various layers and regions are labeled with numbers 1 through 35.

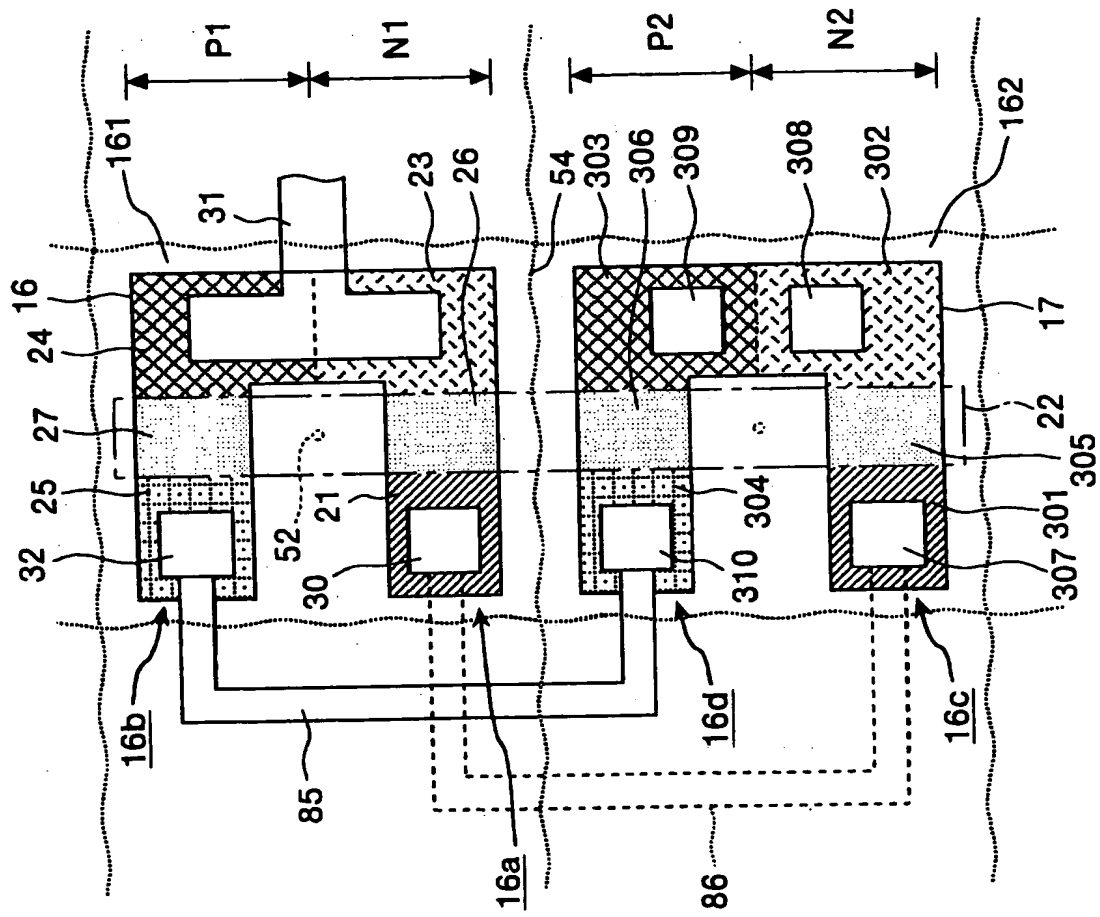
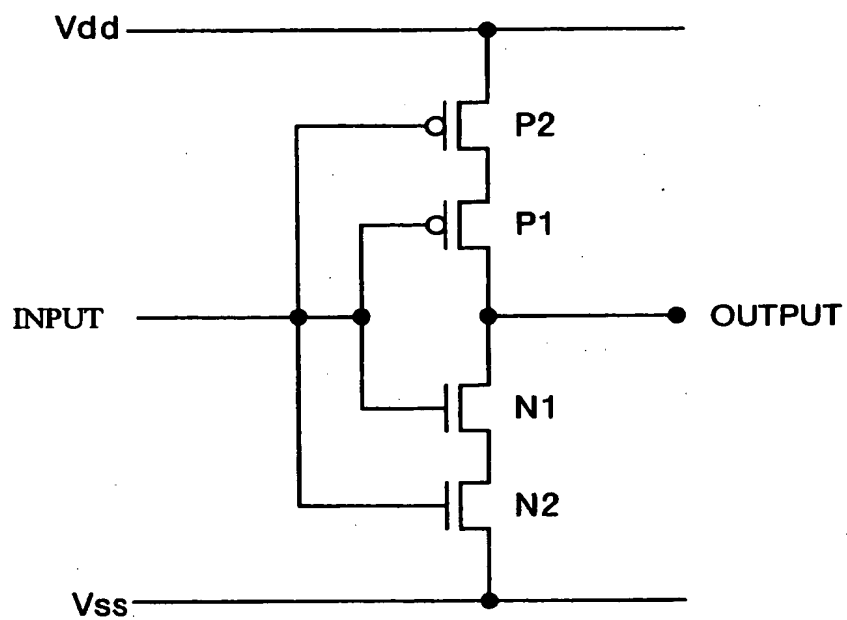


FIG.15



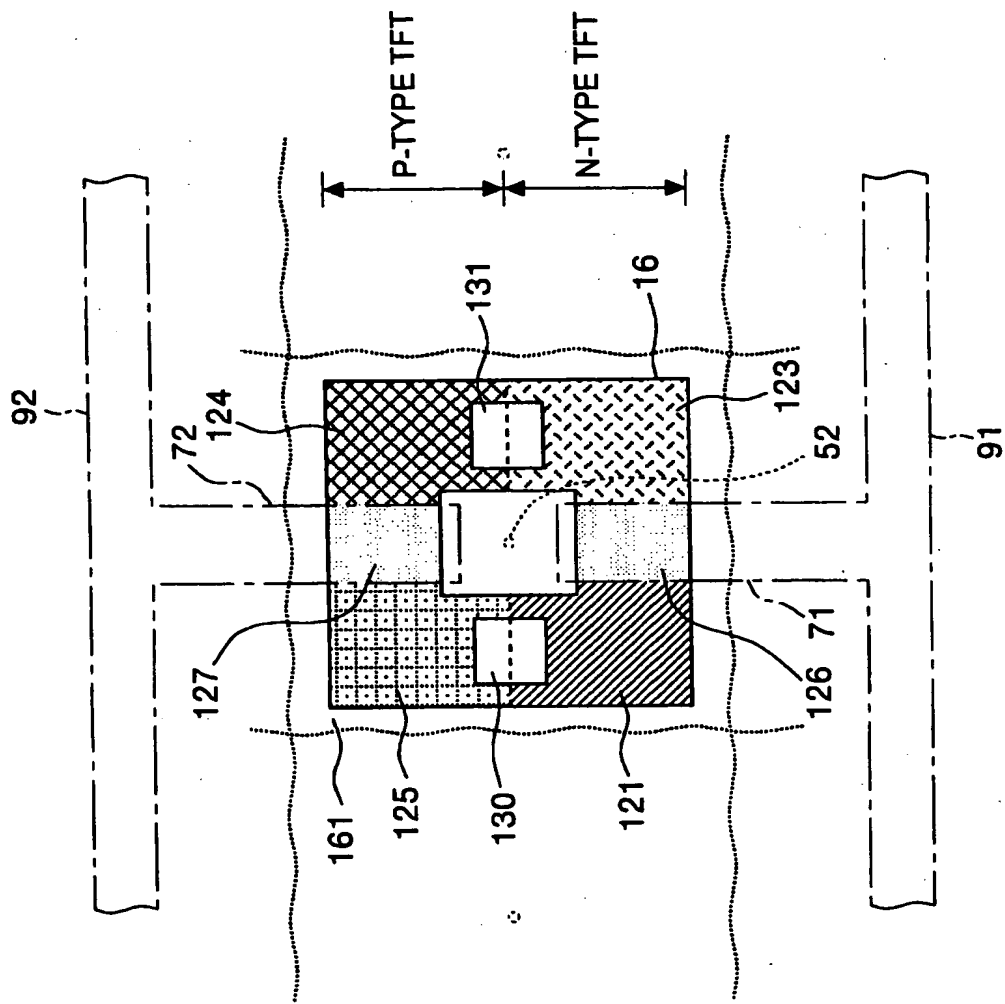


FIG.17

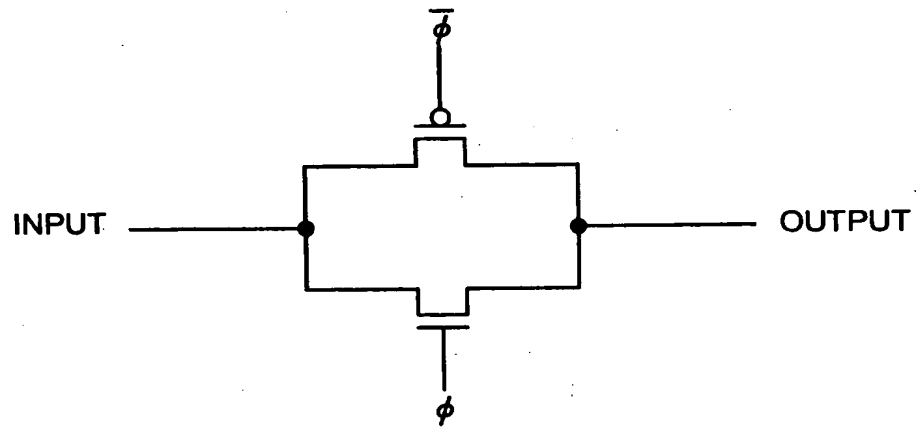


FIG.18

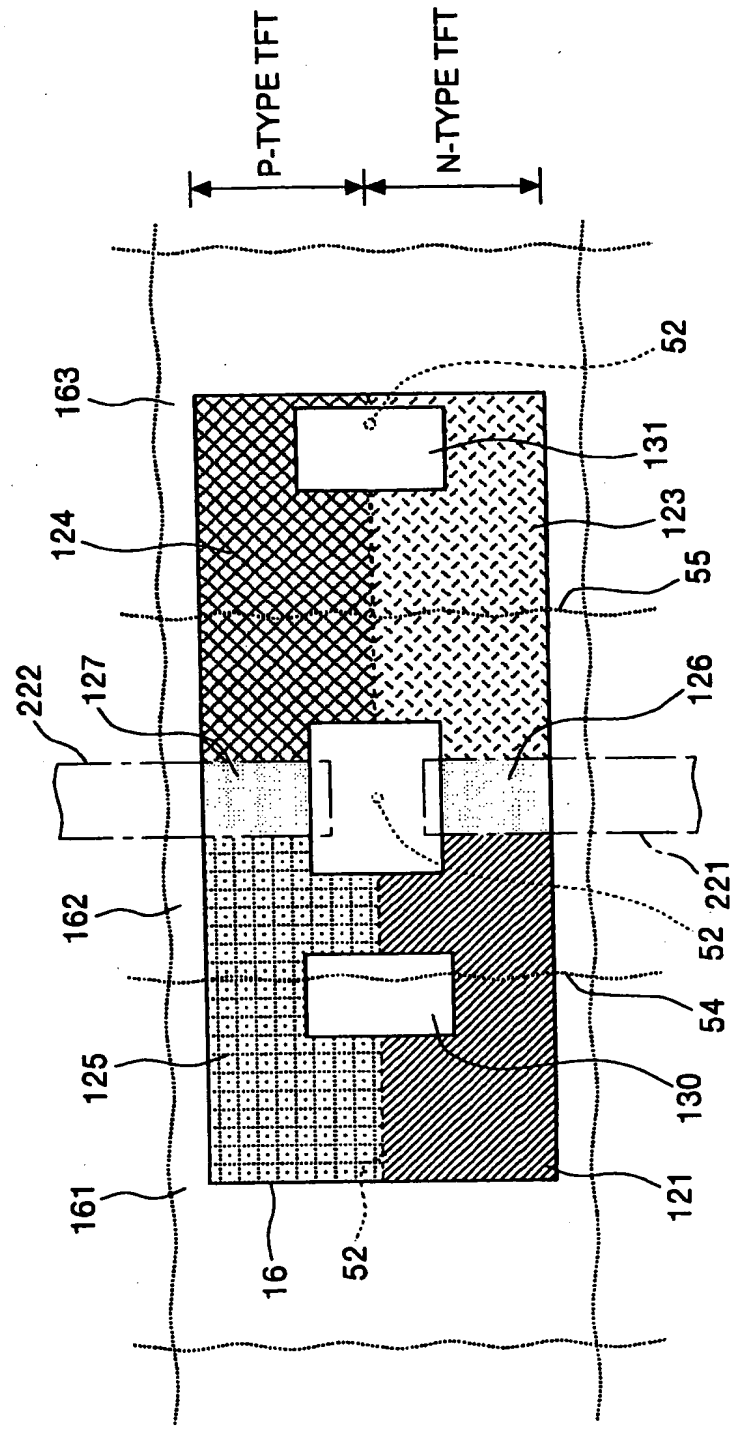




FIG.20

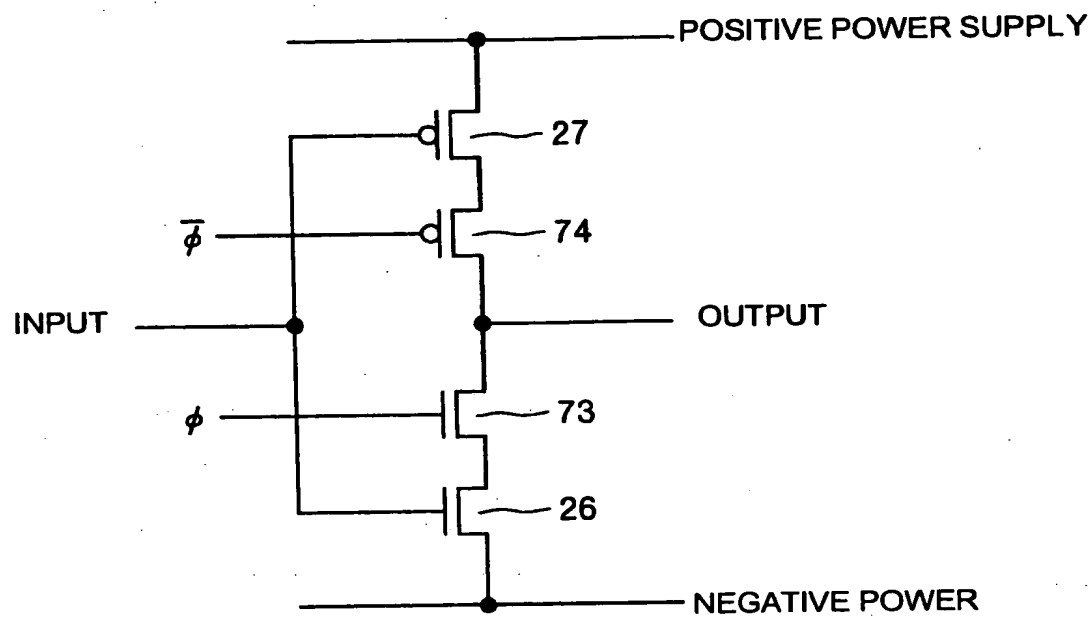




FIG.21

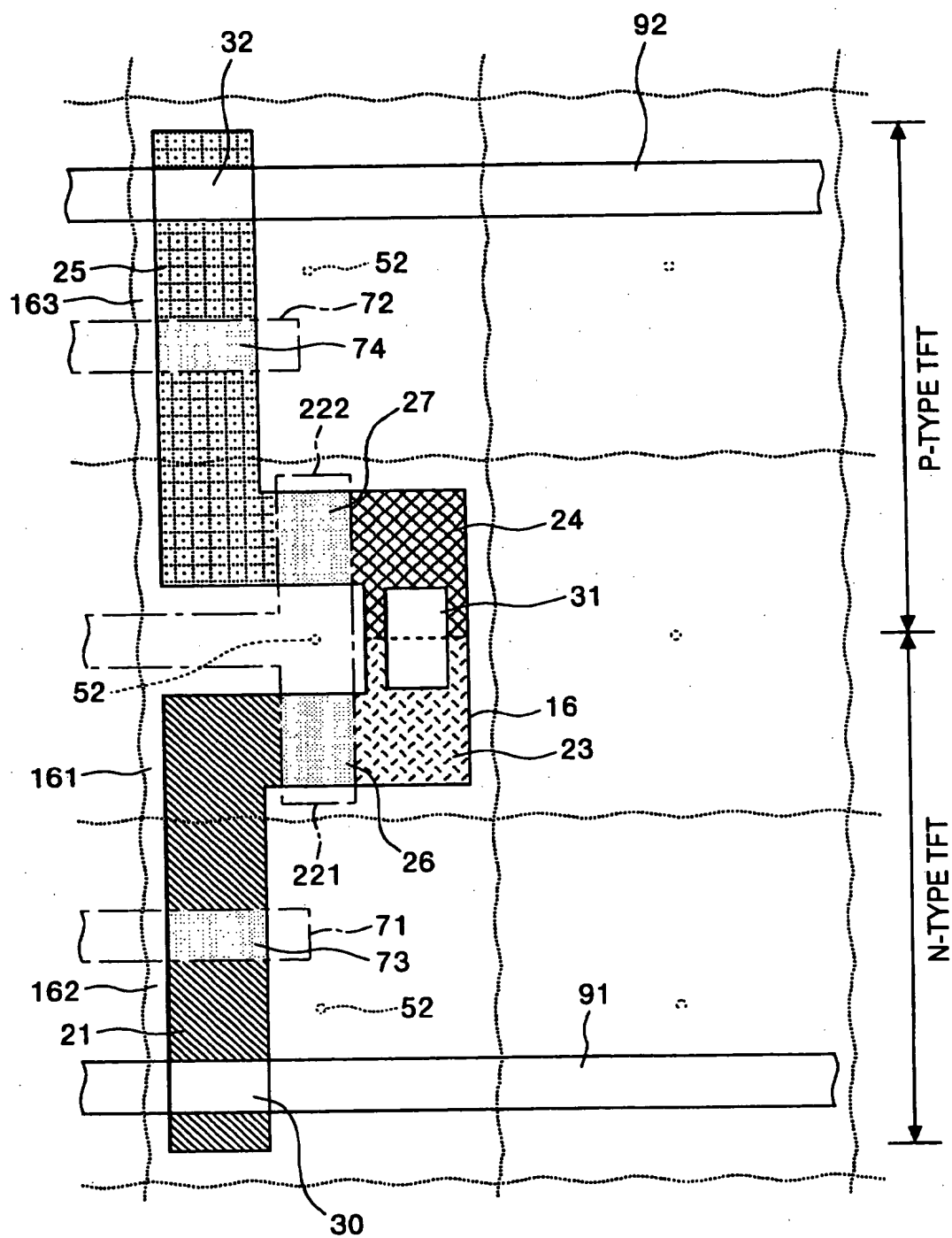


FIG.22

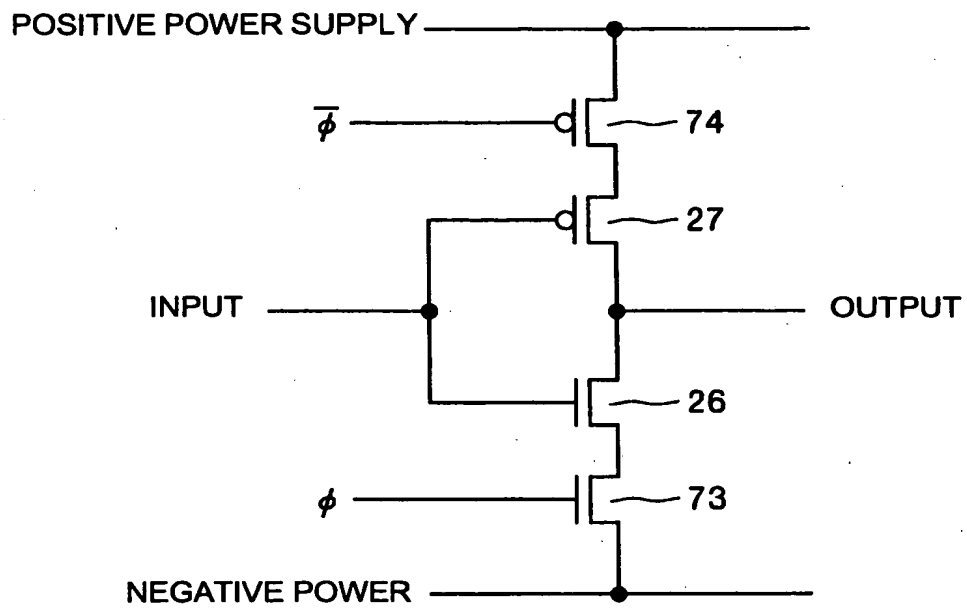


FIG.23

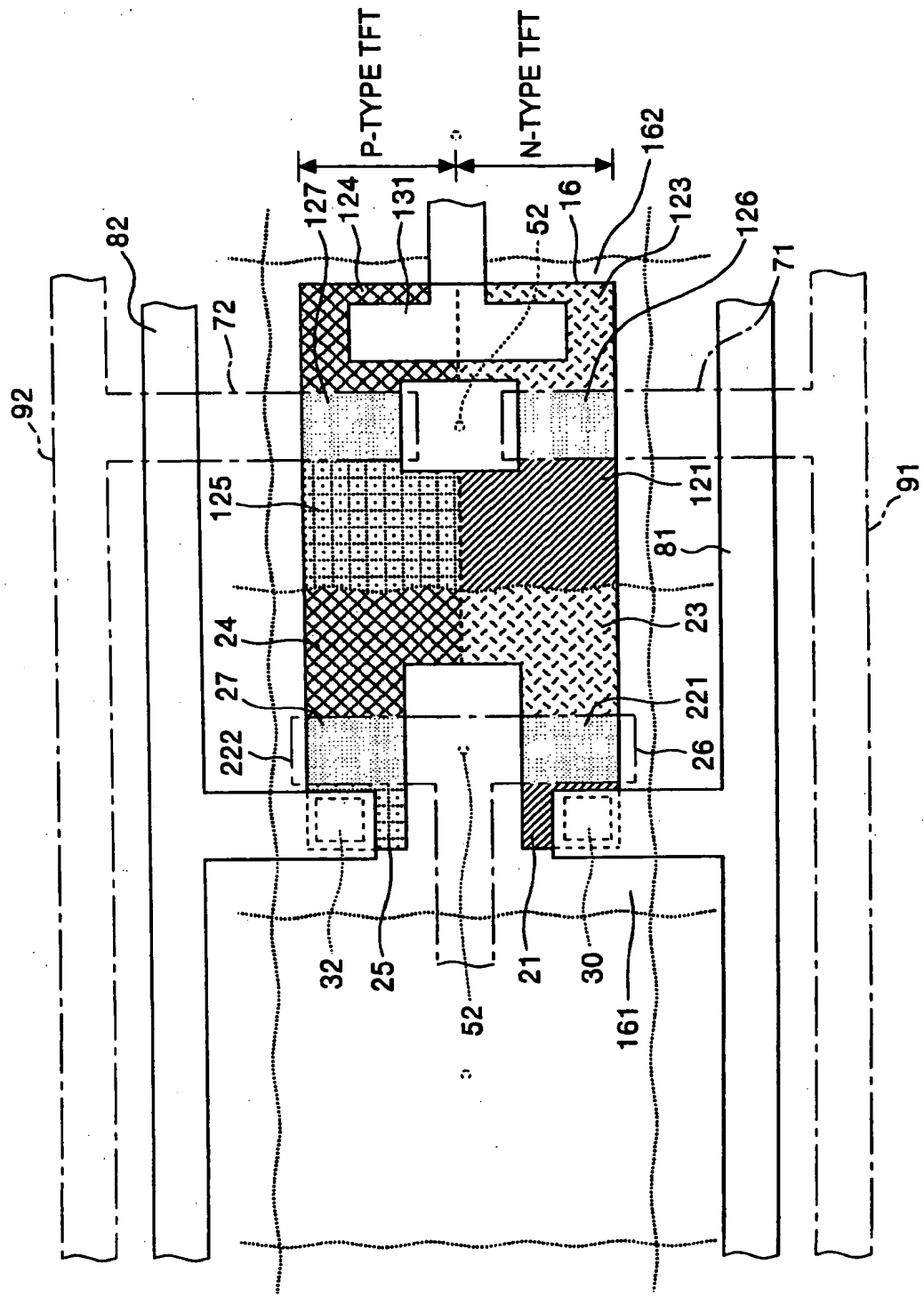


FIG.24

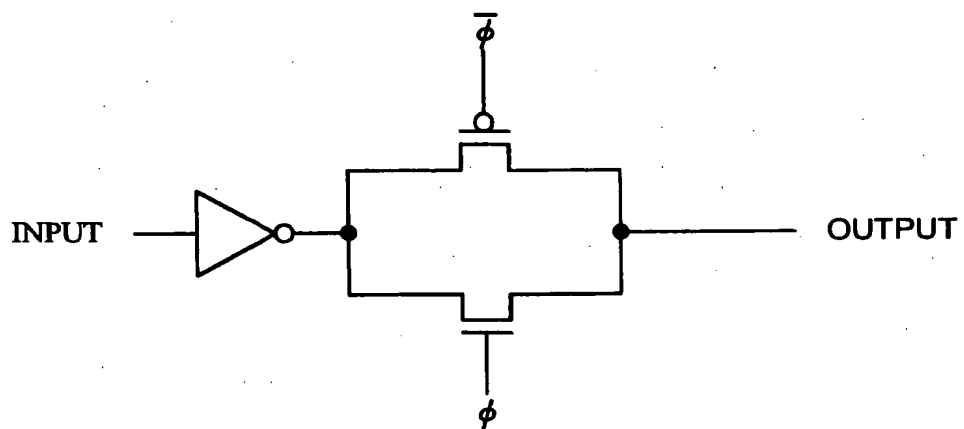
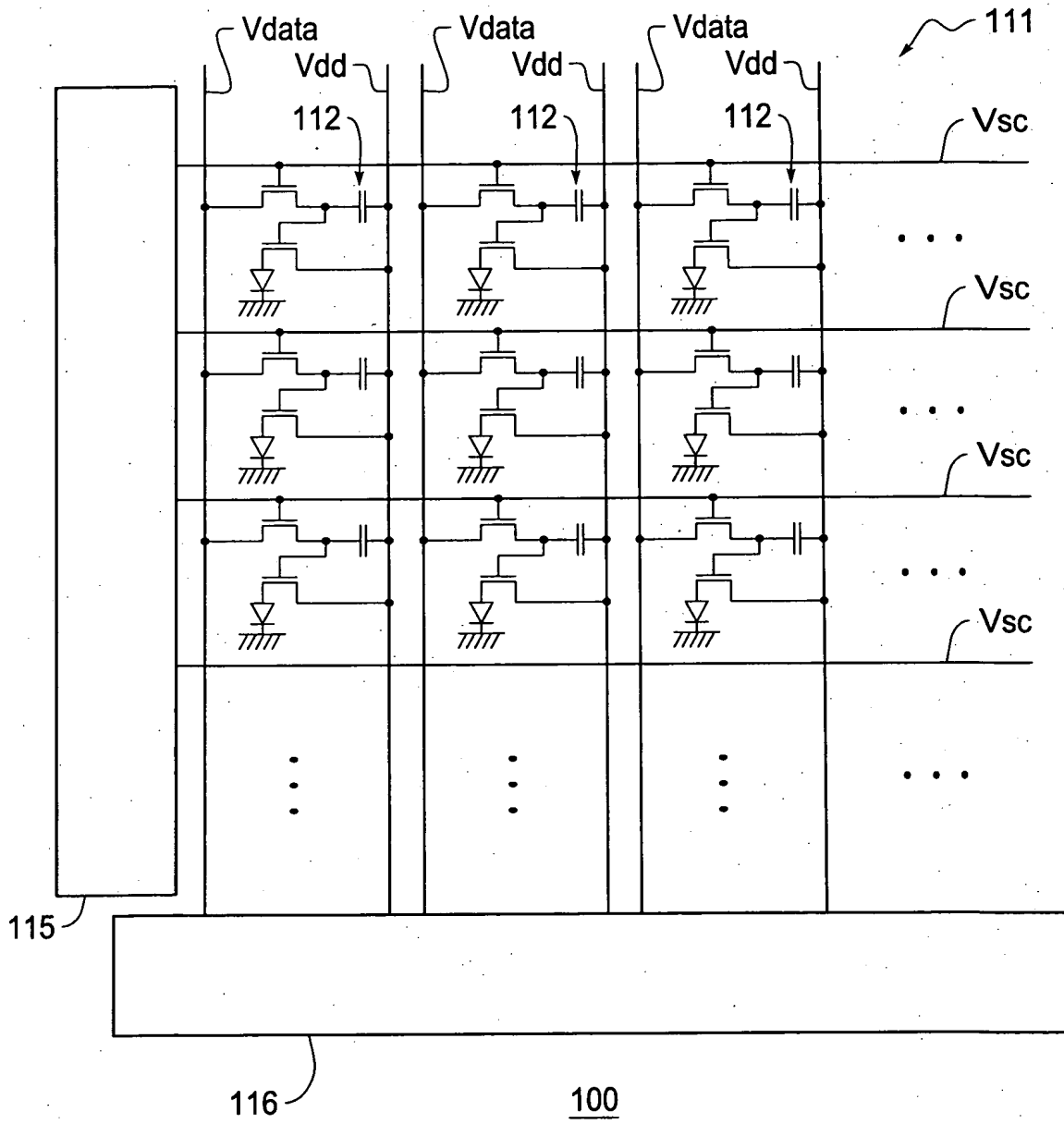


FIG. 25



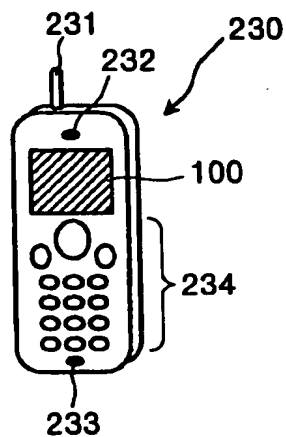


FIG. 26A

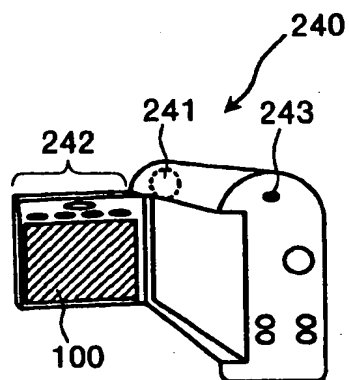


FIG. 26B

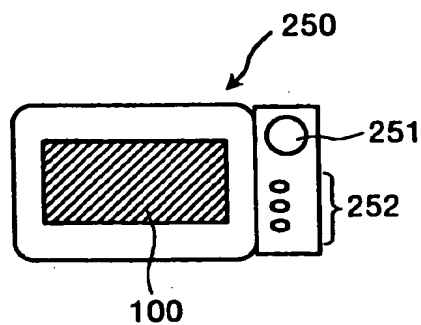


FIG. 26C

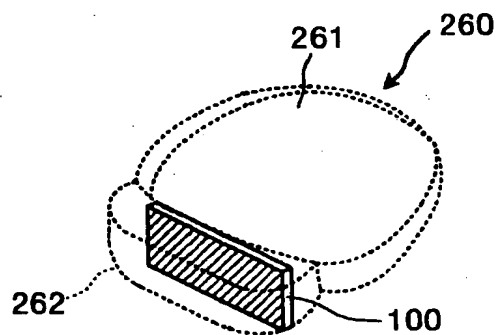


FIG. 26D

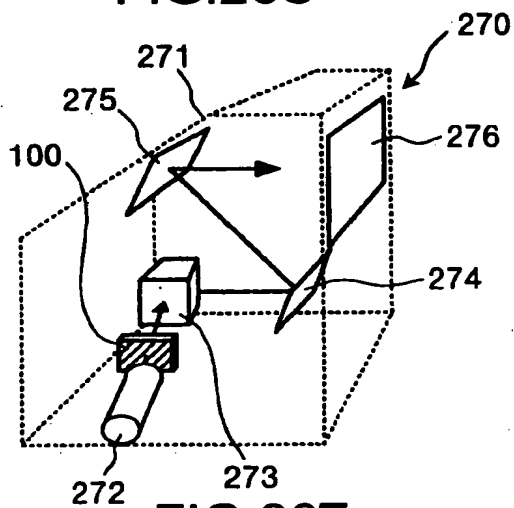


FIG. 26E

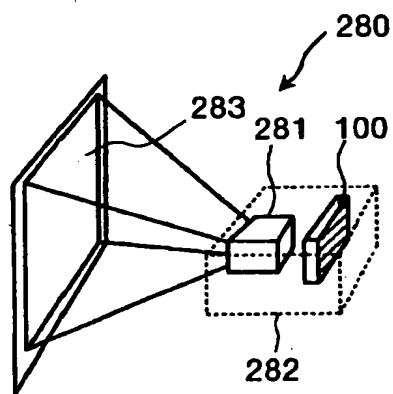


FIG. 26F